REMARKS

Claims 1-17 are in the application. By this amendment, claim 3 has been amended and claims 1,2, and 4-17 remain in original form. Claims 18-22 were canceled without prejudice in response to a requirement for restriction.

REJECTION OF CLAIMS 1, 2, 4-6, AND 8-16 UNDER 35 U.S.C. § 102(b)

Claims 1, 2, 4-6, and 8-16 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,182,225 to Matthews. This rejection is respectfully traversed.

Matthews teaches at column 13, line 40, and continuing to column 16, line 34, that with reference to FIGS. 11A and 11B, after the N-LDD and well compensation implants have been performed, source, drain, emitter (SDE) polysilicon layer 58 is deposited isotropically over the surface of the wafer in a furnace at 580 °C. This is the polysilicon which fills all of the spaces 38 across the wafer. Once again, SDE poly 58 is an amorphous poly layer and is deposited to a thickness of approximately 10,000 Å. Because SDE poly 58 is deposited isotropically, an absolutely uniform deposition takes place on all sides of oxide 57 and above silicon substrate. Uniform deposition rates as well as uniform spacing between polysilicon members insures that previously vacant spaces 38 are filled isotropically. In other words, if the spaces 38 between polysilicon members were nonuniformal or varied in width, then certain regions (narrower spaces) would fill quicker resulting in a nonplanar surface.

After a sufficient thickness of SDE poly 58 is deposited to insure planarization, it is anisotropically (vertically) etched back. This reactive ion etch of SDE poly 58 continues until the tops of the gates are cleared of polysilicon as is shown in FIGS. 12A and 12B. At this stage of the process, SDE poly 58 fills all of the spaces 38 between polysilicon members 33-36. Eventually, SDE poly members 58 will be used to produce the sources, drains, and emitters of the transistors in addition to forming an interconnect layer for the completed circuit. As is clearly seen in FIGS. 12A and 12B, following etch back of SDE poly layer 58 the surface of the wafer is entirely replanarized. ... The next masking step opens the source, drain, and gate regions of n-channel FET 30. All three regions are then implanted with a phosphorous ion implant at 180 KeV with a dose of approximately 3.0×10^{15} atoms/cm^2. This phosphorous ion implant is

depicted in FIGS. 14A and 14B by the arrows 41. Phosphorous is deliberately chosen as the n+ type dopant because of its high diffusivity, i.e., its ability to rapidly distribute atoms throughout the polysilicon members. Other SDE polysilicon members, such as members 78 and 79, which could be used as an interconnect layer may also be doped n-type using implant 41. Once n-channel FET 30 has been implanted with phosphorous, another mask is applied to the wafer to open the area over p-channel FET 40. This p+ implant mask also opens up the base areas of BJT 20 while simultaneously protecting the emitters. Boron, having a relatively high diffusivity, is implanted at 100 KeV and a dose of $3.0x10^{15}$ atoms/cm^2. This p+ implant, shown in FIGS. 14A and 14B by arrows 42, dopes polysilicon members 68, 33, 69, and 35 (forming the source, gate and drain polysilicon members of p-FET 40 and polysilicon base member 35 of BJT 20, respectively) heavily p-type. ... Once the implant sequence 41-43 has been completed, a thermal anneal at 950 °C. in an N_2 atmosphere for 60 minutes is performed. This anneal is what actually forms the transistor junctions in the silicon substrate. During the anneal, the previously implanted dopant diffuses from the overlying polysilicon members down into the substrate. In other words, each of the SDE polysilicon members functions as a separate diffusion source introducing impurities into the underlying substrate to form source, drain, emitter and extrinsic base regions of the respective transistors. This is contrary to conventional methods which rely on either direct ion implantation or direct diffusion from a gaseous impurity source. The present method of utilizing doped polysilicon as a diffusion source provides much better control of diffusion rates and junction depth. The actual junctions formed by this method are characterized as being extremely shallow (necessary for very small device structures) and of a very high quality (resulting in low leakage transistors).

Diffusion from a polysilicon source also provides a novel way to form submicron polysilicon bipolar emitters. As polysilicon emitters provide superior performance in bipolar transistors, this simple doping method is a very valuable processing feature. This is particularly so in the case in a BiCMOS process where submicron polysilicon emitters and very shallow FET junctions are formed simultaneously. Simultaneous diffusion of n-type and p-type dopants into the substrate to form device junctions saves a considerable number of processing steps and obviates the need to subject the wafer to additional heat cycles. ... FIGS. 15A and 15B illustrate a cross section of the wafer following the drive-in (i.e., anneal) of the source/drain, base and emitter regions of FETs 30 and 40 and BJT 20. In detailed summary, source/drain regions 73

and 74 of p-channel FET 40 are formed by diffusion of boron from doped polysilicon members 68 and 69; source/drain regions 75 and 76 of n-channel FET 30 are formed by diffusion of phosphorus from polysilicon members 65 and 66; extrinsic base region 81 is formed by diffusion of boron from doped polysilicon base member 35; and emitter region 77 is formed by diffusion of arsenic from doped polysilicon member 67. In the currently preferred embodiment, the junction depth of regions 73-76 and 81 are on the order approximately 0.17 microns while the junction depth of emitter region 77 is approximately 0.1 micron. Incidentally, the width of emitter region 77 is approximately 0.2 microns in the preferred embodiment of the present invention.

Thus, the single anneal performs two functions: First it distributes the impurities uniformly throughout the polysilicon members. Second, it diffuses those impurities into the silicon substrate to form hypershallow electrical junctions. (Note that in FIGS. 15A and 15B SDE polysilicon member 84 is shown having an associated n-type diffused region 82 directly below it in the silicon substrate. Diffusion region 82 extends down to collector plug 25 to form a low resistance contact with buried layer 13. Although not discussed, SDE polysilicon member 84 is doped n-type using either emitter implant 43 or n-channel FET implant 41).

Matthews' BiCMOS process thus far described provides several unique advantages over prior art processes. To begin with, the invention of Matthews implements a planarization scheme by controlling the spaces etched into a first layer of polysilicon (i.e., waffelization), across the entire surface of the wafer. Once the waffelized spaces have been etched, planarization is achieved by a second deposition of polysilicon (isotropic) followed by an unmasked anisotropic etch. This produces an extremely high degree of planarization which permits extremely small device structures and spacings to be formed.

A second way that Matthews' BiCMOS process achieves narrow device spacing is by the method of using a thin field oxide to overcome the problem of extended birds' beak. The high coupling capacitance, which usually results from the use of thin field oxide, is overcome by the novel metal interconnect scheme.

Planarization is also aided by the use of amorphous polysilicon, which is naturally very smooth and devoid of any grain structure. These properties facilitate reactive ion etching, making it easier to etch accurate features. The use of amorphous polysilicon, lacking any grain structure, also avoids creating nonuniformities or asperities in the underlying crystal. This is of

particular importance in the situation where the polysilicon layer is etched down to the emitter regions of the bipolar transistors.

Thus, Matthews teaches the use of an amorphous polysilicon material, thereby precluding the inclusion of a step for redistributing the polysilicon. What's more, as the passages of Matthews provided herein clearly show, Matthews teaches diffusion of the dopant material, not redistribution of the polycrystalline silicon material. It is respectfully pointed out that diffusion of an impurity material and redistribution of a crystalline structure occur through different mechanisms.

Applicant, on the other hand, teaches on page 5, lines 7-29, of the application that a layer of polysilicon material 132 having a major surface 134 and a thickness ranging from a monolayer of polysilicon to approximately 300 Å is formed on ONO structure 130. By way of example, polysilicon layer 132 is formed using chemical vapor deposition. After deposition, surface 134 has a Root Mean Square (RMS) surface roughness of greater than 75 Å. A void 136 may form during deposition of polysilicon layer 132. Referring now to FIG. 5, semiconductor component 100 is annealed in a hydrogen (H_2) ambient to redistribute or reposition the silicon atoms of polysilicon layer 132 and form a void-free polysilicon layer 138 having a smoothed surface 140 and a thickness of less than about 300 Å. Redistribution of the silicon atoms fills void 136 and any other void that may have formed in polysilicon layer 132 and smoothes surface 134 such that it has an RMS surface roughness that is preferably less than about 50 Å and even more preferably less than about 20 Å. To distinguish the smooth-surfaced, void-free electrically conductive layer from electrically conductive layer 132 that contains voids and has a rough surface, reference numbers different from 132 and 134 have been used to identify the electrically conductive layer and its surface, respectively. In particular, reference 138 has been used to identify the annealed polysilicon layer and reference number 140 has been used to identify its surface which is smooth. By way of example, polysilicon layer 132 is annealed at a temperature ranging from about 750 degrees Celsius (°C) to about 1,100 °C, a pressure ranging from about 10 Pascals (Pa) to about 40 kiloPa, and a time ranging from about 5 seconds to about 60 minutes. The parameters for annealing polysilicon layer 132 (e.g., temperature, pressure, and time) are not a limitation of the present invention.

Accordingly, applicants' claim 1 calls for, among other things, forming a first polysilicon layer over the first and second surface features and redistributing the first polysilicon layer in at

least the region between the first and second surface features. Applicants' claim 9 calls for, among other things, forming a first layer of polysilicon over the first and second conductors and repositioning atoms of the first layer of polysilicon. At least these limitations of applicants' claims 1 and 9 are not included in the relied on reference of Matthews. Because all limitations of claims 1 and 9 are not included in the relied on reference of Matthews, it cannot anticipate applicants' claims 1 and 9.

Claims 2, 4-6, and 8 depend either directly or indirectly from claim 1 and are believed allowable over the relied on reference of Matthews for at least the same reasons as claim 1. Claim 2 further sets out that redistributing the first polysilicon layer comprises annealing the first polysilicon layer. Claim 6 further sets out redistributing the second polysilicon layer. At least these limitations of claims 2 and 6 are not included in the relied on reference of Matthews, further precluding the anticipation of claims 2 and 6.

Claims 10-16 depend either directly or indirectly from claim 9 and are believed allowable over the relied on reference of Matthews for at least the same reasons as claim 9. Claim 12 further sets out that repositioning atoms of the first layer of polysilicon comprises annealing the first layer of polysilicon. Claim 13 further sets out that repositioning atoms of the first layer of polysilicon comprises heating the first layer of polysilicon to a temperature of at least 750 degrees Celsius. At least these limitations of claims 12 and 13 are not included in the relied on reference of Matthews, further precluding the anticipation of claims 12 and 13.

REJECTION OF CLAIMS 3, 7, AND 17 UNDER 35 U.S.C. § 103(a)

Claims 3, 7, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,182,225 to Matthews in view of the remark. This rejection is respectfully traversed.

Claims 3 and 7 depend either directly or indirectly from claim 1 and are believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 1.

Claim 17 depends from claim 9 and is believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 9.

As discussed hereinbefore, Matthews does not teach or suggest redistributing or repositioning atoms of polycrystalline silicon, but rather teaches the diffusion of dopant atoms in a semiconductor material. In addition, Matthews does not teach or suggest redistributing or repositioning atoms of polycrystalline silicon in a hydrogen ambient. Matthews merely teaches in column 17, line 60, and continuing to column 18, line 2, that a hydrogen alloy at 400 °C. in forming gas (15% H_2+85% N_2) is performed next to introduce hydrogen (H_2) into the isolation regions of the circuit. Hydrogen is intentionally introduced to reduce the surface state charge density, Q_{SS}. Normally, in prior art processes, this step is done very late in the process. However, because all of the regions defined up to this point will soon be encased in a nitride layer (which is impenetrable to H_2) the isolation oxide regions are loaded with hydrogen at this point in the process.

Applicant, on the other hand, teaches the redistribution or repositioning of a polycrystalline structure. Accordingly, applicants' claim 3 further sets out that redistributing the first polysilicon layer comprises annealing the first polysilicon layer in an ambient comprising hydrogen. Claim 7, further sets out that redistributing the second polysilicon layer includes annealing the second polysilicon layer in a hydrogen ambient. Claim 17 further sets out that repositioning atoms of the first layer of polysilicon includes repositioning the atoms in an ambient comprising hydrogen. At least these limitations of applicants' claims 3, 7, and 17 are not included in the relied on references, either alone or in combination, further precluding obviousness of claims 3, 7, and 17.

It is respectfully submitted that by teaching that amorphous polysilicon, is naturally very smooth and devoid of any grain structure which facilitates reactive ion etching, making it easier to etch accurate features and further teaching that the use of amorphous polysilicon, lacking any grain structure, also avoids creating nonuniformities or asperities in the underlying crystal, Matthews teaches away from applicants' limitation of redistributing or repositioning the polysilicon material. A rejection of claims under 35 U.S.C. §103(a) is improper when the references teach away from applicants' claimed invention. There is no motivation to redistribute or reposition the polysilicon atoms because Matthews teaches using a material that avoids creating nonuniformities or asperities in the underlying crystal. Because there is no motivation, suggestion, or teaching of redistributing or repositioning the polysilicon atoms, the relied on

references, either singly or in combination, are deficient in making obvious applicants' claims 3, 7, and 17.

Because the amorphous polysilicon surface of Matthews is already smooth, there is no reason for Matthews to consider smoothing it further by redistributing or repositioning atoms of the polycrystalline silicon, further showing that Matthews does not teach or suggest redistributing or repositioning atoms of the polycrystalline silicon.

CONCLUSION

No new matter is introduced by the amendments herein. Based on the foregoing, applicants believe that all claims under consideration are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,

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